Compiler-enabled Power-Efficient Register File Protection

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Abstract:

Register file (RF) is extremely vulnerable to soft errors, and traditional redundancy based schemes to protect the RF are prohibitive not only because RF is often in the timing critical path of the processor, but also since it is one of the hottest blocks on the chip, and therefore adding any extra circuitry to it is not desirable. Software approaches would be ideal in this case, but previous approaches that are based on program duplication have very significant runtime overheads, and others based on instruction scheduling are only moderately effective due to local scope.

This talk will be about how compiler alone and in conjunction with microarchitecture can power-efficiently protect the RF. What we have observed is that a significant portion of the RF vulnerability is contributed by long lifetime variables. Protecting only these can result in power-efficient RF protection. Thus the task of the compiler is to identify program variables that have long lifetimes and protect them. Our experiments demonstrate pure compiler techniques can reduce the vulnerability of the RF by 33-37% on average and up to 66%, with a small (2%) runtime overhead. As compared to hardware protection mechanisms, compiler analysis can achieve the same level of protection but at 25% lesser RF energy consumption.